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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER

TM02/0604

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ART UNIT

PAPER NUMBER

2151

DATE MAILED:

06/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/127,085

Applicant(s)

Paul E. McKenney

Examiner

Majid A. Banankhah

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— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Mar 22, 2001

2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-6 is/are pending in the application

4a) Of the above, claim(s) _____ is/are withdrawn from consideration

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-6 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirements

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. _____.
- ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

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1. This final office action is in response to paper number 4, response which was received June 19, 2000. Applicant's argument have been fully considered but they are not deemed to be persuasive. Claims 1-6 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior Office action.

3. Claims 2-6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. For example the preamble of claim 2 recite "physical memory", and "data structure". There is no relationship between any of these elements and the means or steps of the claims. It is not clear whether "physical memory" in line 14 is the same as "memory" in line 17. It is unclear "the data structure" on line 15, stores a number of current generation of its node or number of current generation for every other node (See the next statement: "data structure comprising a variable stored in the memory of each node and ..."). Is this data structure unique for all the nodes or every node has its own data structure storing the number of current generation of all the nodes including

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itself. As another example, in claim 3, line 25, the data structure on a processor determines if all other processor's node have passed through a quiescent state, then in line 27, the claim recite "indicating in a data structure accessible to all nodes". Is it the same data structure recited on line 25, which could determine if all other processors on its node have passed through a quiescent state. If so, the step on line 27-29 is the repeat of the previous step.

Claims 4-6 are rejected because of the rejection of their parent claims.

4. Claims 1-6 are rejected under 35 U.S.C. § 103 as being unpatentable over Slingwine (U.S.Pat No. 5,727,209) in view of Roche et al. (U.S.Pat No. 4,916,697).

As per claim 1-3, Slingwine, teaches:

- of **multi processor** (See Abstract, **multi processor**, col. 2, lines 8-19), having **interconnected processing nodes** (Fig. 3, **elements 108, and 110**), **states of threads** (Fig. 3, elements 112, also **summary of thread activity**, col. 8, lines 31-41), mutual exclusion between current and next generation data elements (**mutual exclusion overhead, and a generation data structure**, col. 7, lines 18-46).

While the reference of Slingwine teaches of existence of a

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quiescent state when it is known that the thread will not be accessing data structures protected by mutual exclusion mechanism, he fail to explicitly teaches of bit masks for indication of whether a processor has passe through a quiescent state. However, it is well known in the art at the time invention was made to use level bit mask for the indication of passing through a quiescent state, as it is evidenced by Roche et al. (Each bit in the sculpture register 72 has an associated bit in two or three mask register, ...Col. 8, line 5-30). Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use "level bit mask registry as an indication of a state of a processor" of Roche, in the multi exclusion and concurrency method of Slingwine et al.

Regarding claims 4-6 and the limitation of callback processor checking is the processor has passed through a quiescent state and indicating that in the data structure, the reference of Slingwine et al. teaches of **A CALLBACK PROCESSOR 100**, and **A CALLBACK PROCESSOR 104** which is an element of a generation data structure, and an entity that monitors a summary of thread activity 106 (col. 6, lines 36-50).

5. Applicant on page 3 of his argument argue "As discussed below, the combination suggested by the Examiner fails to

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encompass first and second level bits masks comprising a data structure, as recited in claim 1 [See office action, p.5]. The suggested combination therefore does not contain all the elements of claim 1". Later on page 4, a pplicant argue "The combination of Slingwine and Roche fails to teach or suggest, on a multi processor computer system with "multiple interconnected processing nodes" a data structure as recited in claim 1 with a "first level bit mask" for node data and "second level bit mask[s]" for processors within a node data". In response, first it must be pointed out that every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. **In re Bode**, 550 F.2d 656, 193 USPQ 12 (CCPA 1977). Secondly, applicants attention is respectfully directed to fig.1B where processors are all connected to form computer [10], and the computer is connected to a network. Later Slingwine teaches of a hierarchical per-thread bitmap in col. 9, lines 31-44. In there, he teaches of a per thread bitmap which is a data structure in which at the lowest level maintains one bit per thread and at the next level up maintains one bit per group of threads. Later in col. 18, lines 33-43, he teaches of the fact that the implementation has a system wide scope preferably uses a hierarchical per-thread bitmap, per level generation counters, a **global generation counter**, and a counter to track the execution histories of a possible large number of processes.

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Later on page 4, last paragraph, applicant argue "Nor would there be any motivation to combine the references as suggested by the Examiner. As discussed above, the structure recited in claim 1 is not shown by the primary reference, Slingwine. The secondary reference, Roche is completely unrelated and recites partitioned clock stopping in response to processing errors. The references are completely unrelated and applicant respectfully requests the Examiner to point to where any motivation to combine these two disparate references can be found. MPEP 706.02 (j) and 2143.01. Applicant believe no motivation to combine exists". In response it is submitted that the test for obviousness under 35 USC 103 is not the express suggestion of the claimed invention in any or all of the references but what the references taken collectively would suggest. **In re Conrad**, 169 USPQ 170 (CCPA 1971). One cannot show non-obviousness by attacking the references individually where the rejection is based on a combination of references. **In re Young**, 159 USPQ 725 (CCPA 1968). The reference of Roche is used to show that "level bit mask registry can be used as an indication of a state of a processor", and this is clearly explained in the 103 rejection [see section 4 of this office action].

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6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE application has been amended as follows: ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Maid A. Banankhah** whose voice telephone number is (703) 308-6903. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:
Commissioner of Patent and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist).
All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the

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Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Maid Banankhah

June 1, 2001


MAJID A. BANANKHAH
PRIMARY EXAMINER